REMARKS

The Office Action dated April 2, 2004 has been received and carefully noted. The above amendments to the claims and the following remarks are submitted as a full and complete response thereto.

Claim 6 has been amended to more particularly point out and distinctly claim the invention. No new matter has been added, and no new issues are raised which require further consideration and/or search. Claims 1-7 are submitted for consideration.

Claim 6 was objected to because of informalities. Claim 6 has been amended. Therefore, Applicant requests that the objection be withdrawn.

Claims 1-3, 6, and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,243,497 to Chiang et al. The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claims 1 and 7.

Claim 1, upon which claims 2-6 depend, recites a method for synchronization adaptation of asynchronous digital data streams. The method includes the steps of providing a first digital data stream (PCM_IN) at a first sample rate (CLK_1) and

inputting the first digital data stream (PCM_IN) to a sample rate conversion means (SRC). The method also includes the steps of supplying data output from the sample rate conversion means (SRC) to a processing element (BUFFER) and storing the supplied data into the processing element (BUFFER). The method further includes the step of

outputting the data stored in the processing element as a second digital data stream (PCM_OUT) at a second sample rate (CLK_2), with the first and the second sample rates (CLK_1, CLK-2) being different from each other. The method is characterized by the further steps of detecting a state (BUFFER_STATUS) of the processing element (BUFFER) and controlling the sample rate conversion means (SRC) dependent on the detected state of the processing element.

Claim 7 recites a device for synchronization adaptation of asynchronous digital data stream. The device includes a sample rate conversion means (SRC) to which is input a first digital data stream (PCM_IN) at a first sample rate (CLK_1). The device also includes a processing element (BUFFER) for storing data output from the sample rate conversion means (SRC) and for outputting the data stored in the processing element as a second digital data stream (PCM_OUT) at a second sample rate (CLK_2), with the first and the second sample rates (CLK_1, CLK_2) being different from each other. The device is characterized by a detection means for detecting a state (BUFFER_STATUS) of the processing element (BUFFER) and a control means for controlling the sample rate conversion means (SRC) dependent on the detected state of the processing element.

As outlined below, Applicant submits that the cited reference of Chiang et al. does not teach or suggest the elements of claims 1-7.

Chiang et al. teaches an apparatus for deriving a quantizer scale for each frame to maintain the overall quality of a video image which controls the coding rate. Col. 2, lines 36-39. An input video image on a signal path is received into a motion estimation

module for estimating motion vectors. Col. 2, line 61-Col. 3, line 12. The use of motion vectors enhances image compression by reducing the amount of information transmitted on a channel because only the changes between the current and reference frames are coded and transmitted. Col. 3, lines 8-22. The motion vectors from the motion estimation module are received by a motion compensation module for improving the efficiency of the prediction of sample values. Col. 3, lines 23-26. Prior to performing motion compensation prediction, a coding mode must be selected and the motion compensation module generates a motion compensated prediction image on a path of the contents of the block based on past and/or future reference pictures. This motion compensation prediction on the path of the contents is subtracted via a subtractor from the video image on the signal path to form an error signal or predictive residual signal. Col. 3, lines 37-54. A DCT module then applies a forward discrete cosine transform process to each block of the predictive residual signal to produce a set of 8x8 block of DCT coefficients. The resulting 8x8 block is received by the quantization module where the DCT coefficients are quantized, thereby reducing the accuracy with which the DCT coefficients are represented by dividing the DCT coefficients by a set of quantization values with appropriate round to form integer values. Col. 3, line 60-Col. 4, line 4. Since a different quantization value can be applied to each DCT coefficient, a quantization matrix is generally established as a reference table and the encoder chooses a quantization matrix that determines how each frequency coefficient in the transformed block is quantized. Col. 4, lines 15-22.

The resulting 8x8 block of quanitzed DCT coefficients is received by a variable length coding model where the two dimensional block is scanned in a "zig-zag" order to convert it into a one dimensional string of quantized DCT coefficients. Col. 4, lines 39-44. The data stream is receiving in a FIFO buffer. The rate control module monitors and adjusts the bit rate of the data stream entering the FIFO buffer to prevent overflow and underflow on the decoder side after transmission of the data stream. Thus, it is the task of the rate control module to monitor the status of the buffer to control the number of bits generated by the encoder. The rate control module selects a quantizer scale for each frame to maintain the overall quality of the video image while controlling the coding rate. Vol. 4, line 51-Col. 5, line 9.

The Office Action seems to suggest that Chiang et al. teaches inputting the first digital data stream to a sample rate conversion means as recited in claims 1 and 7 as transmitting an input video image on a signal path into a motion estimation module for estimating motion vectors. The Office Action also seems to suggest that Chiang et al. teaches supplying data output from the sample rate conversion means to a processing element as recited in claims 1 and 7 as applying a forward discrete cosine transform process to each block of the predictive residual signal to produce a set of 8x8 block of DCT coefficients. The Office Action also seems to suggest that Chiang et al. teaches outputting the data stored to the processing element as a second digital data stream at a second sample rate, with the first and the second sample rates being different from each other as recited in claims 1 and 7 as receiving the resulting 8x8 block and converting it

into a one dimensional string of quantized DCT coefficients which is received in a FIFO buffer, wherein the rate control module monitors and adjusts the bit rate of the data stream entering the FIFO buffer to prevent overflow and underflow on the decoder side after transmission of the data stream. However, the columns of Chiang et al. cited by the Office Action does not teach or suggest the steps of detecting a state of a processing element and controlling the sample rate conversion means dependent on the detected state of the processing element as recited in claims 1 and 7. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. § 102(e) rejection should be withdrawn because Chiang et al. simply does not teach or suggest each element of claims 1 and 7 and hence dependent claims 2-6.

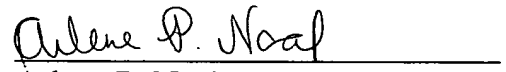
Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang et al. because the Office Action states that Chiang et al. fails to explicitly teach "disabled if the detected state has the third value." However, the Office Action states that one skilled in the art would have been motivated to disable the "coding rate" adjustment by the control module because one such adjustment was needed. As noted above, Chiang et al. fails to disclose or suggest detecting a state of a processing element and controlling the sample rate conversion means dependent on the detected state of the processing element as recited in claims 1 and 7. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. § 103(a) rejection be withdrawn because Chiang et al. simply does not teach or suggest each element of claims 1 and 7 and hence claims 4 and 5.

As noted previously, claims 1-7 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 1-7 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802
APN:lls